Chung Yuan Journal, Vol. 30, No. 3 / 2002, September / p. 373-375

A CMOS Rail-to-Rail 1.5-Volt Fully Differential Opamp

CHUN-LI HOU AND CHIH-WEI CHIANG

Department of Electronic Engineering
Chung Yuan Christian University
Chung-Li, 32023,Taiwan, R.O.C.

(Received: December 18, 2001; Accepted: January 28, 2002)

ABSTRACT

The CMOS rail-to-rail fully differential Opamp has an input stage and a class AB output stage, which can provide both input and output rail-to-rail operations. Its input stage is composed of an NMOS differential pair and a PMOS differential pair. HSPICE simulation results are preformed using level 49 model of a 0.5μm CMOS process. This Opamp has a dc gain of 66dB, a unity-gain bandwidth of 2.1MHz and a phase margin of 64°.

Key words: *CMOS, Rail-to-Rail, Fully Differential Opamp.*

I. Introduction

Recently the demand for even smaller and cheaper electronic chip in electronic system has guided the manufacturers to integrate entire systems on a single chip. Analog cells applied in digital systems must operate at low voltage and low power dissipation.

Various methods have been used to design low-voltage analog circuits. Some of these methods are: (a) modifying the fabrication process to reduce the threshold voltages of MOS transistors, (b) multiplying the external supplied voltage on the chip, and(c) using innovative circuit design techniques. The first method results in higher fabrication cost for a multiple V technology, the second method suffers from problems of reliability. So it seems that the best approach is to tolerate the existing technologies, which are mainly developed in digital applications.

In this paper, a 1.5-volt only, CMOS rail-to-rail fully differential Opamp is presented. The input stage is composed of an NMOS differential pair and a PMOS differential pair, which can be used to achieve rail-to-rail operation. While the rail-to-rail output operation is realized by using a class AB output stage. HSPICE simulation results are performed using level 49 model of a 0.5μm CMOS process. Besides, the ±1.5V power supply can be obtained by employing two batteries.

II. Rail-to-rail fully differential Opamp operation

(a) Two Differential Pair Input Stage

To realize rail-to-rail operations, two differential pairs are used to provide a rail-to-rail operation at both Vp and Vn terminals. Transistors M1 and M2 conduct till the positive supply rail, and transistors M3 and M4 conduct till the negative supply rail. In terms of the concept of current mirrors, the conducting currents are summed at the drains of transistors M1 and M2 as shown in Fig. 1.

(b) Class AB Output Stage

The class AB amplifier can provide and receive current with the load. Consequently, it is faster and more power-efficient than the class A amplifier is. Furthermore, the rail-to-rail output operation can be obtained through the class AB output stage.

Crossover distortion can be virtually eliminated by biasing the complementary output transistors at a small voltage. The level-shift circuit with appropriate transistor types, is used to drive the output transistors. The utilized output stage is the best one among all the class AB output stages since the difference between the gate voltages of the output transistors remains constant.

Fig. 2 is a class AB output stage of this rail-to-rail fully differential Opamp.

(c) Whole CMOS Rail-to-Rail Fully Differential Opamp

Fig. 3 illustrates the whole schematic diagram of the rail-to-rail fully differential Opamp.

III. Simulation result

The simulation results of the frequency response for this circuit are shown in Fig. 4. Compare with the data in the other columns of table1 which are given in the reference [5]. It is obvious that the Opamp proposed in this paper is better than the one given in reference [5], especially for the bandwidth and the slew rate. The output loading is 5pF.

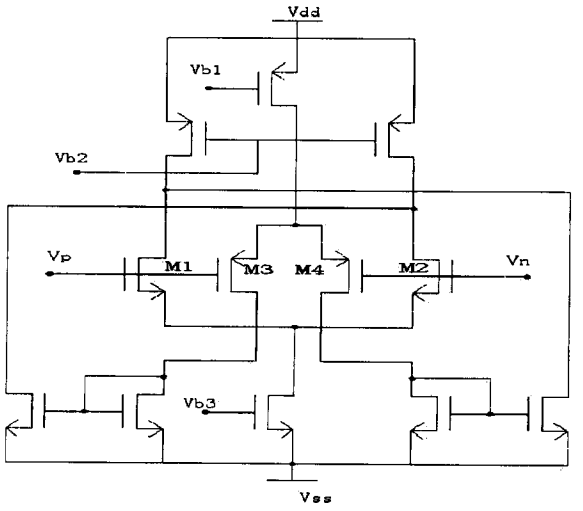

Fig. 1 The rail-to-rail input stage

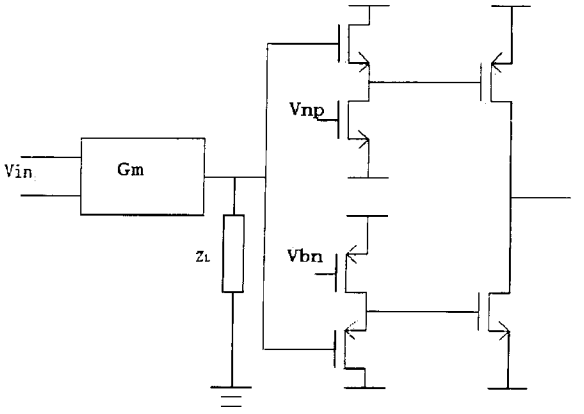

Fig. 2 The class AB output stage

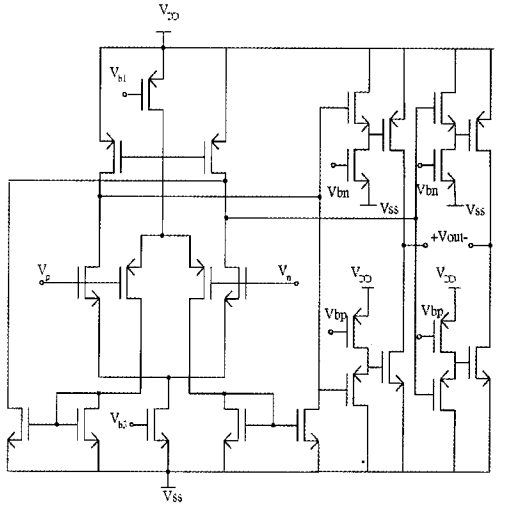

Fig. 3 The complete Opamp circuit

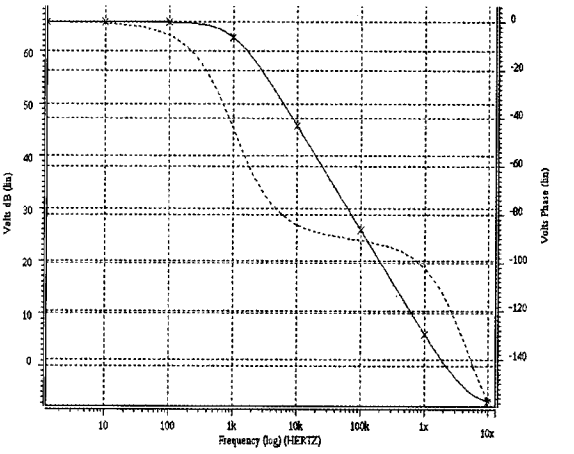

Fig. 4 Frequency response of the designed Opamp

Table 1

	This work	[5]
supply	1.5	1.5
DC Gain(dB)	66dB	65dB
GBW(MHz)	2.1MHz	300KHz
PM(degree)	64	80
SR(V/μs)	2.51	0.4

IV. Conclusion

Simulation results of the rail-to-rail fully differential Opamp are obtained, while its class AB output stage

is utilized to achieve higher speed and swing.

HSPICE simulation results are preformed using level 49 model of a 0.5μm CMOS process. It owns the following characteristics: DC gain of 66dB, unity-gain bandwidth of 2.1MHz, and phase margin of 64°.

References

1 Faramarz Bajmani and S.M. Fakhraie, "A Rail-to-rail 1-Volt CMOS Opamp", *IEEE Int. Symp. Circuits and System*, 217-219, 1997.

2 Coban A.L. and Allen G., "A 1.75 V rail-to-rail CMOS Opamp," *IEEE Int. Symp. Circuits and System*, 497-500, 1994.

3 Gabriel A. Rincon-Mora, "A Low Voltage, Rail-to-Rail, Class AB COMS Amplifer With High Drive and Low Output Impedance Characteristics," *IEEE Transaction and system-II: Analog And Digital Signal Processing*, Vol. 48, 753-761,2001.

4 Johns David A. and Martin Ken, Analog integrated circuit design, Wiley, 1997.

5 Behzad Razavi, Design of Analog CMOS Integrated Circuits, Mc GrawHill, 2001.

一個用 CMOS 軌對軌 1.5V 全差動運算放大器

侯 俊 禮　　江 致 緯

中原大學電子工程學系

中壢市普仁 22 號

摘 要

這個具有一輸入級與AB類輸出級之CMOS rail-to-rail 全差動運算放大器，它可提供輸入與輸出 rail-to-rail 運算。其輸入級是由一組 NMOS 差動對與一組 PMOS 差動對所組成。而HSPICE模擬結果是以0.5μm CMOS/Level 49 Model的製程參數所得到的。此運算放大器具有66dB的直流增益，2.1 MHz的單一增益頻寬及 64 度的相位邊限。

關鍵詞：CMOS ，軌對軌，全差動運算放大器。